AMENDMENTS TO THE ABSTRACT

Please delete the section entitled "ABSTRACT OF THE DISCLOSURE" in its entirety and substitute the following section therefor:

ABSTRACT OF THE DISCLOSURE

A microprocessor that includes an instruction cache indexed by a fetch address is disclosed. The instruction cache caches instructions and provides the instructions to an instruction buffer for storage therein. The instructions comprise variable byte-length instructions. The microprocessor also includes a branch target address cache, coupled to the instruction buffer and indexed by the fetch address, which caches branch target addresses of previously executed branch instructions. The instruction buffer includes an indicator associated with each byte of each of the instructions stored in the instruction buffer. The indicator has a true value if the branch target address cache predicts that the byte is an opcode byte of one of the instructions and that the instruction is one of the previously executed branch instructions and the microprocessor has speculatively branched to one of the branch target addresses cached for the previously executed branch instruction.